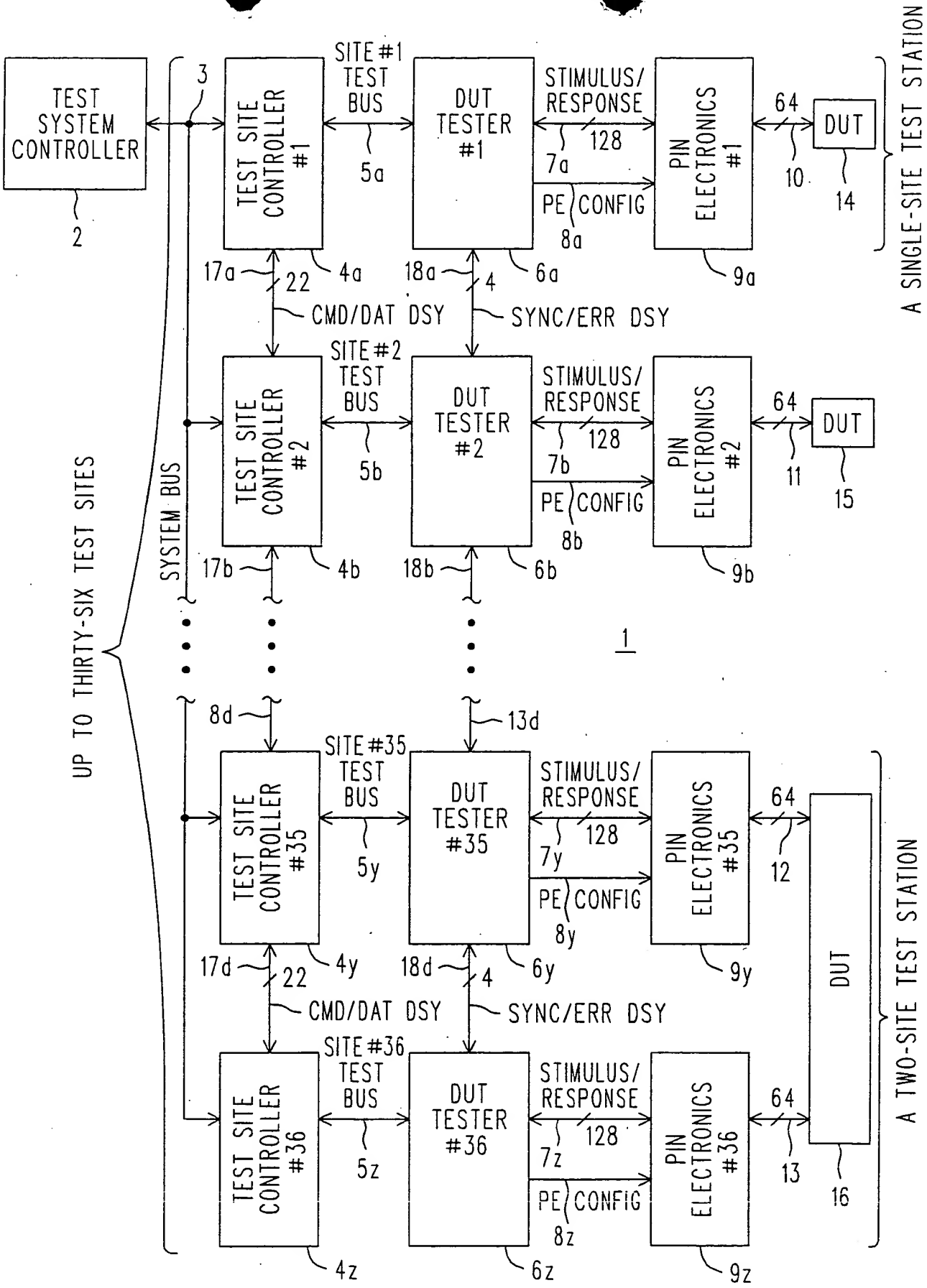

TEST SYSTEM CONTROLLER
2
3
TEST SITE CONTROLLER #1
SITE #1 TEST BUS
5a
DUT TESTER #1
STIMULUS/ RESPONSE
128
7a
PE CONFIG
8a
PIN ELECTRONICS #1
64
DUT
10
14
A SINGLE-SITE TEST STATION
17a
22
4a
18a
4
6a
9a
CMD/DAT DSY
SYNC/ERR DSY
TEST SITE CONTROLLER #2
SITE #2 TEST BUS
5b
DUT TESTER #2
7b
8b
PIN ELECTRONICS #2
11
15
17b
4b
18b
6b
9b
SYSTEM BUS
UP TO THIRTY-SIX TEST SITES
1
8d
13d
TEST SITE CONTROLLER #35
SITE #35 TEST BUS
5y
DUT TESTER #35
7y
8y
PIN ELECTRONICS #35
12
17d
4y
18d
6y
9y
TEST SITE CONTROLLER #36
SITE #36 TEST BUS
5z
DUT TESTER #36
7z
8z
PIN ELECTRONICS #36
13
16
4z
6z
9z
A TWO-SITE TEST STATION

FIG. 1

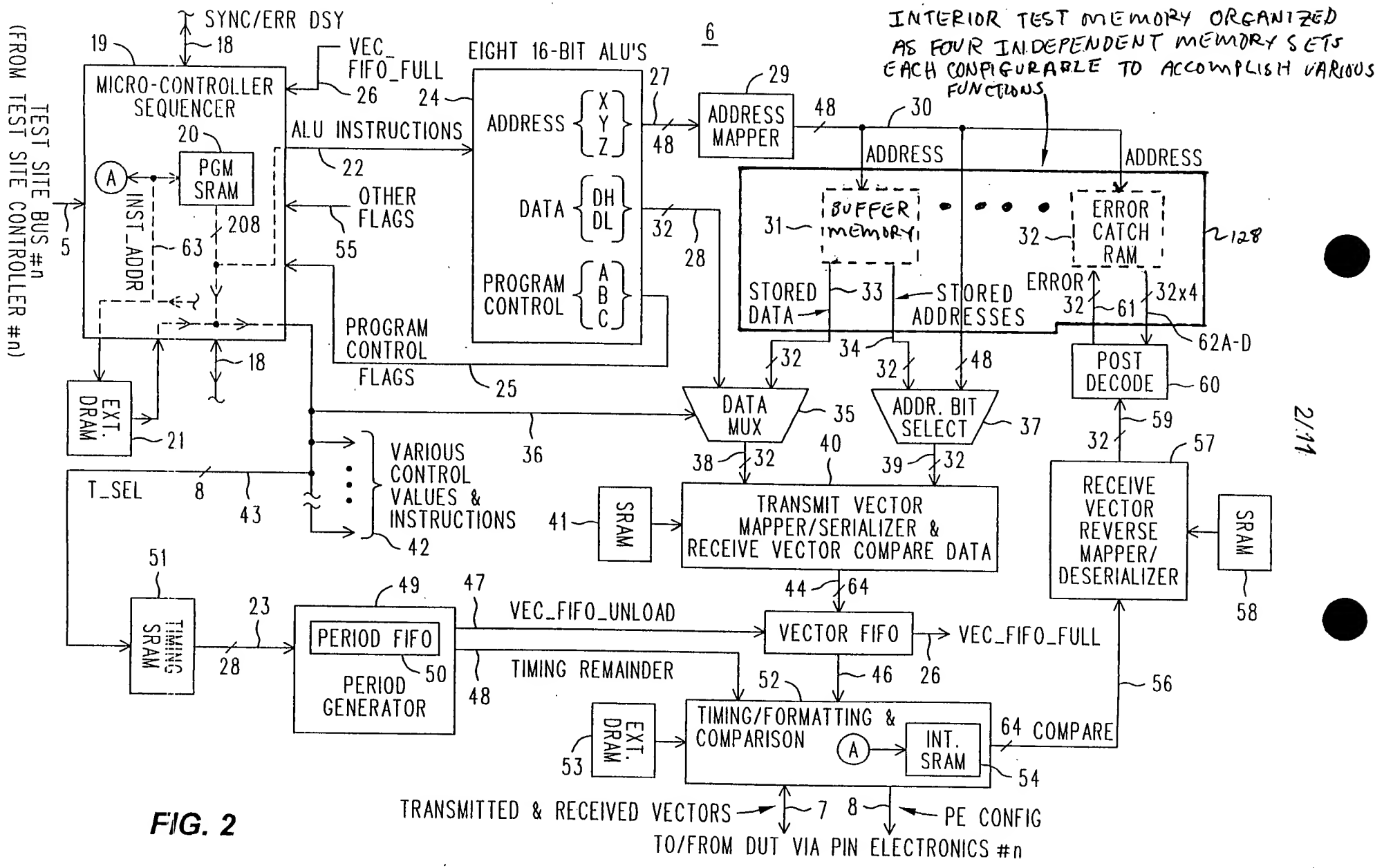

SYNC/ERR DSY
18
19
MICRO-CONTROLLER SEQUENCER
20
PGM SRAM
INST_ADDR
63
208
5
TEST SITE BUS #n (FROM TEST SITE CONTROLLER #n)
VEC_ FIFO_FULL
26
ALU INSTRUCTIONS
22
OTHER FLAGS
55
PROGRAM CONTROL FLAGS
25
18
EXT. DRAM
21
EIGHT 16-BIT ALU'S
6
24
ADDRESS
X
Y
Z
DATA
DH
DL
PROGRAM CONTROL
A
B
C
27
48
28
32
29
ADDRESS MAPPER
48
30
INTERIOR TEST MEMORY ORGANIZED AS FOUR INDEPENDENT MEMORY SETS EACH CONFIGURABLE TO ACCOMPLISH VARIOUS FUNCTIONS
ADDRESS
ADDRESS
31
BUFFER MEMORY
32
ERROR CATCH RAM
128
STORED DATA
33
STORED ADDRESSES
ERROR
32
32x4
61
62A-D
34
32
48
POST DECODE
60
59
DATA MUX
35
ADDR. BIT SELECT
37
36
VARIOUS CONTROL VALUES & INSTRUCTIONS
42
T_SEL
8
43
38
32
40
39
32
41
SRAM
TRANSMIT VECTOR MAPPER/SERIALIZER & RECEIVE VECTOR COMPARE DATA
44
64
RECEIVE VECTOR REVERSE MAPPER/ DESERIALIZER
32
57
SRAM
58
51
TIMING SRAM
23
28
49
47
PERIOD FIFO
50
PERIOD GENERATOR
48
VEC_FIFO_UNLOAD
TIMING REMAINDER
VECTOR FIFO
VEC_FIFO_FULL
46
26
52
56
EXT. DRAM
53
TIMING/FORMATTING & COMPARISON
INT. SRAM
54
64 COMPARE
TRANSMITTED & RECEIVED VECTORS
7
8
PE CONFIG
TO/FROM DUT VIA PIN ELECTRONICS #n

FIG. 2

2/11

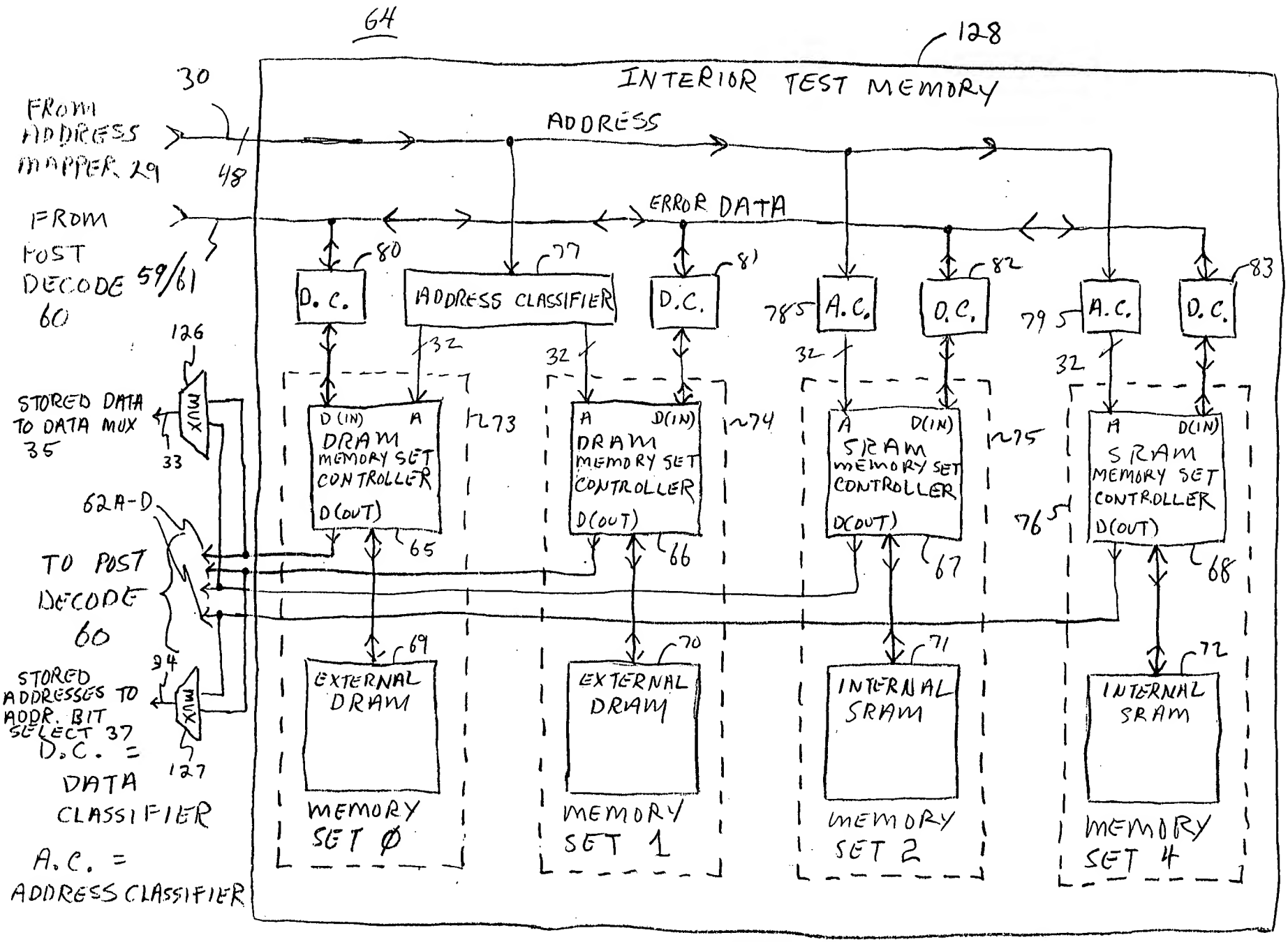

64
128
INTERIOR TEST MEMORY
30
FROM ADDRESS MAPPER 29
48
ADDRESS
ERROR DATA
FROM POST DECODE 59/61 60
80
77
81
82
83
D. C.
ADDRESS CLASSIFIER
D. C.
78
A. C.
D. C.
79
A. C.
D. C.
126
32
32
32
32
STORED DATA TO DATA MUX 35
MUX
33
D (IN)
A
DRAM MEMORY SET CONTROLLER
D(OUT)
73
A
D(IN)
DRAM MEMORY SET CONTROLLER
D(OUT)
74
A
D(IN)
SRAM MEMORY SET CONTROLLER
D(OUT)
75
A
D(IN)
SRAM MEMORY SET CONTROLLER
D(OUT)
76
62A-D
TO POST DECODE 60
65
66
67
68
34
STORED ADDRESSES TO ADDR. BIT SELECT 37
MUX
127
D.C. = DATA CLASSIFIER
A.C. = ADDRESS CLASSIFIER
69
70
71
72
EXTERNAL DRAM
EXTERNAL DRAM
INTERNAL SRAM
INTERNAL SRAM
MEMORY SET Ø
MEMORY SET 1
MEMORY SET 2
MEMORY SET 4

FIGURE 3

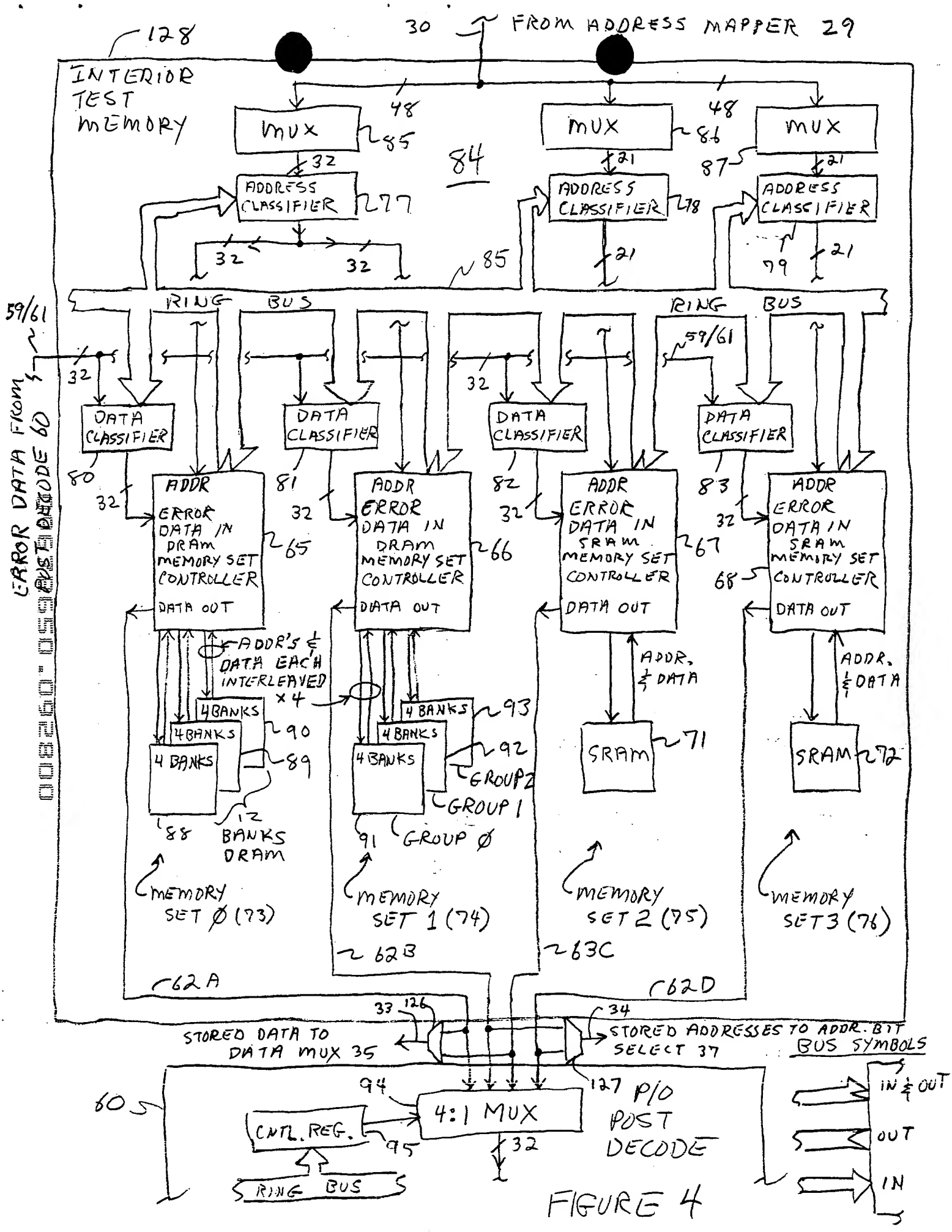

128
INTERIOR TEST MEMORY
30
FROM ADDRESS MAPPER 29
MUX
85
MUX
86
MUX
87
48
48
84
32
21
21
ADDRESS CLASSIFIER
77
ADDRESS CLASSIFIER
78
ADDRESS CLASSIFIER
79
32
32
21
21
85
RING BUS
RING BUS
59/61
59/61
32
32
DATA CLASSIFIER
80
DATA CLASSIFIER
81
DATA CLASSIFIER
82
DATA CLASSIFIER
83
ADDR ERROR DATA IN DRAM MEMORY SET CONTROLLER
65
ADDR ERROR DATA IN DRAM MEMORY SET CONTROLLER
66
ADDR ERROR DATA IN SRAM MEMORY SET CONTROLLER
67
ADDR ERROR DATA IN SRAM MEMORY SET CONTROLLER
68
DATA OUT
DATA OUT
DATA OUT
DATA OUT
ERROR DATA FROM POST DECODE 60
ADDR'S & DATA EACH INTERLEAVED
x4
4 BANKS
4 BANKS
4 BANKS
4 BANKS
4 BANKS
4 BANKS
90
89
93
92
GROUP 2
GROUP 1
GROUP 0
88
12 BANKS DRAM
91
ADDR. & DATA
ADDR. & DATA
SRAM
71
SRAM
72
MEMORY SET 0 (73)
MEMORY SET 1 (74)
MEMORY SET 2 (75)
MEMORY SET 3 (76)
62B
63C
62A
62D
33
126
34
STORED DATA TO DATA MUX 35
STORED ADDRESSES TO ADDR. BIT SELECT 37
BUS SYMBOLS
IN & OUT
OUT
IN
60
94
4:1 MUX
127 P/O POST DECODE
CNTL. REG.
95
32
RING BUS

FIGURE 4

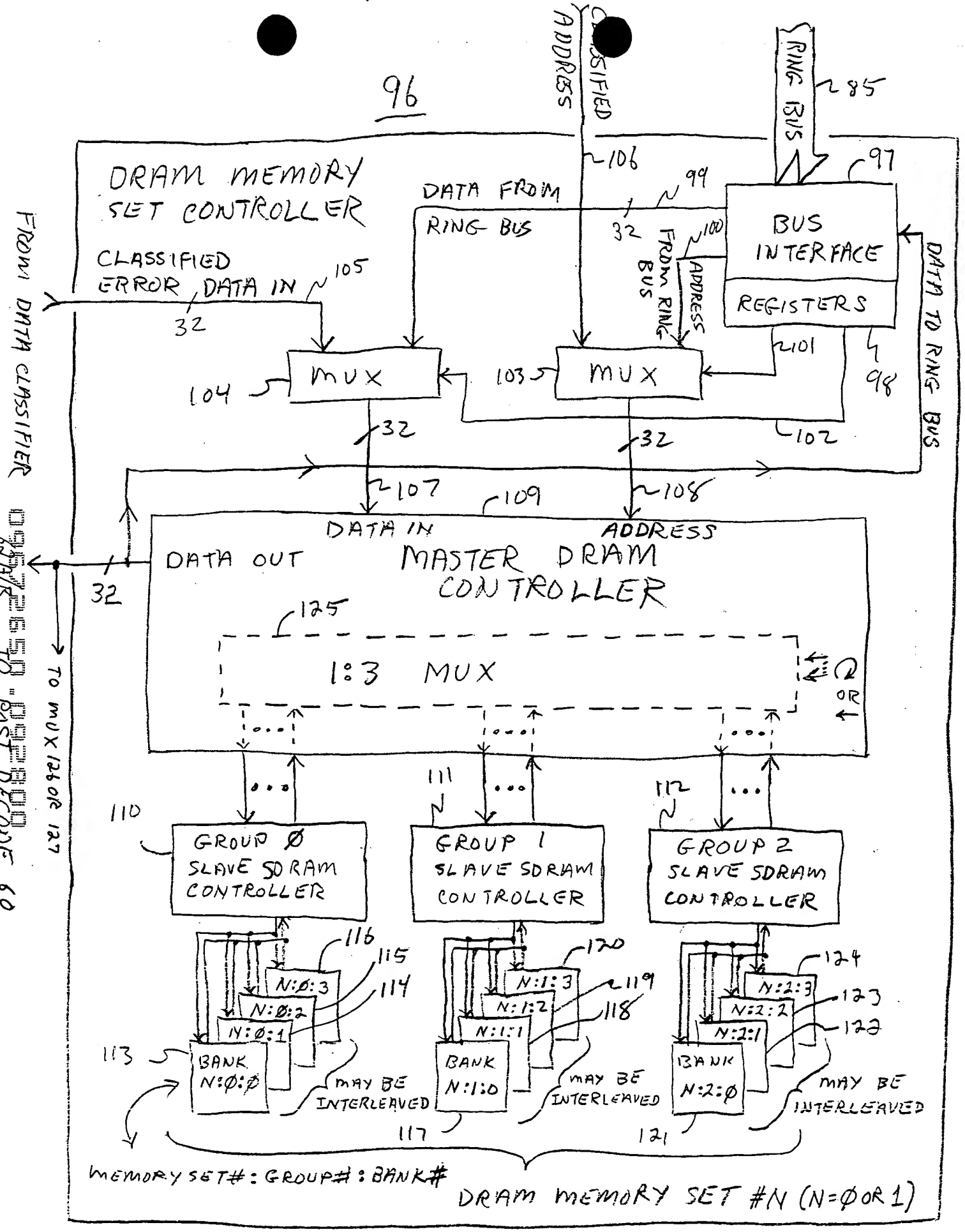

96
DRAM MEMORY SET CONTROLLER
CLASSIFIED ADDRESS
RING BUS
85
106
97
99
DATA FROM RING BUS
32
100
FROM RING BUS
ADDRESS
BUS INTERFACE
REGISTERS
DATA TO RING BUS
CLASSIFIED ERROR, DATA IN
105
32
FROM DATA CLASSIFIER
MUX
104
MUX
103
101
98
102
32
32
107
109
108
DATA IN
ADDRESS
DATA OUT
MASTER DRAM CONTROLLER
32
125
1:3 MUX
OR
TO MUX 126 OR 127
DRAM REQUEST TO "POST DECODE" 60
110
111
112
GROUP Ø SLAVE SDRAM CONTROLLER
GROUP 1 SLAVE SDRAM CONTROLLER
GROUP 2 SLAVE SDRAM CONTROLLER
116
115
114
N:Ø:3
N:Ø:2
N:Ø:1
113
BANK N:Ø:Ø
MAY BE INTERLEAVED
120
N:1:3
N:1:2
N:1:1
119
118
BANK N:1:Ø
MAY BE INTERLEAVED
124
N:2:3
N:2:2
N:2:1
123
122
BANK N:2:Ø
MAY BE INTERLEAVED
117
121
MEMORY SET#: GROUP#: BANK#
DRAM MEMORY SET #N (N=ØOR1)

FIGURE 5

ADDRESS CLASSIFIERS (77, 78, 79)
(X32 FOR 77, X21 FOR 78, 79)

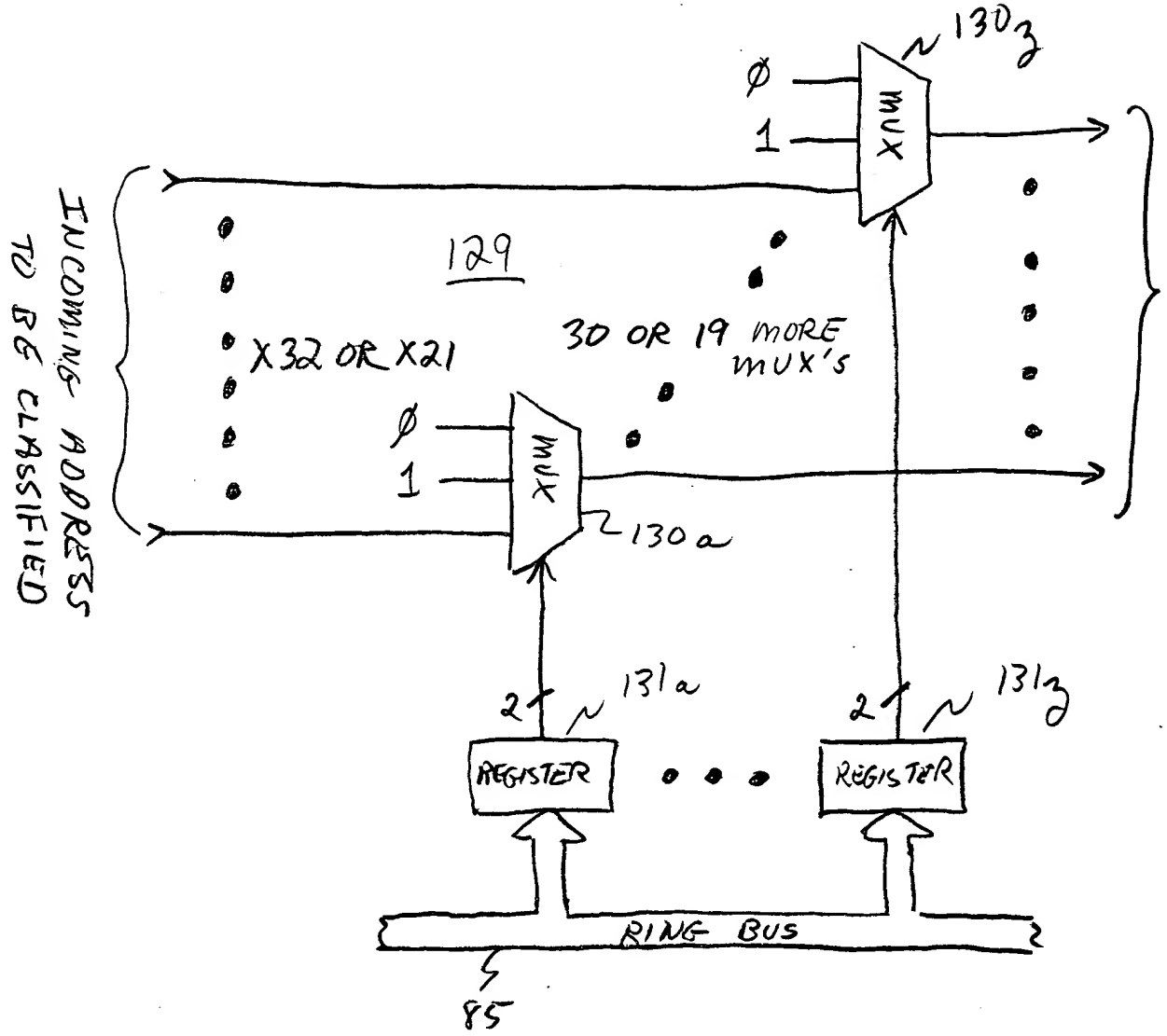


FIGURE 6

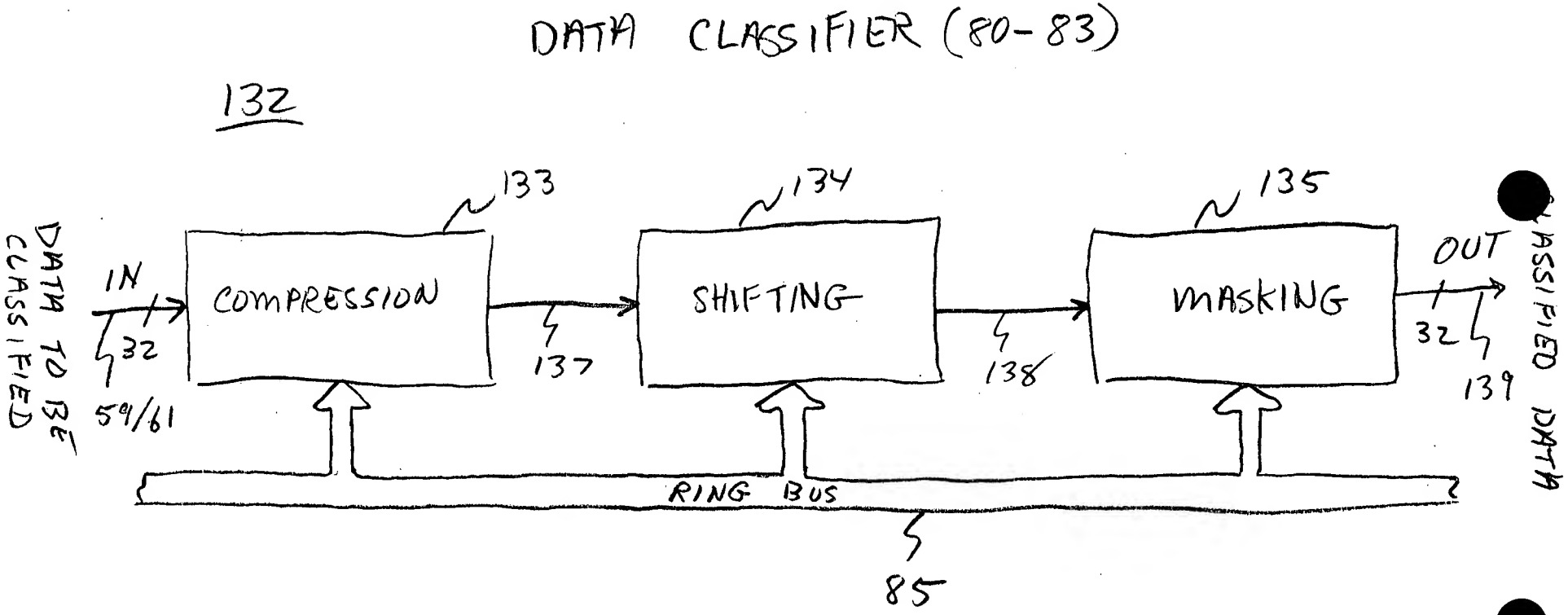
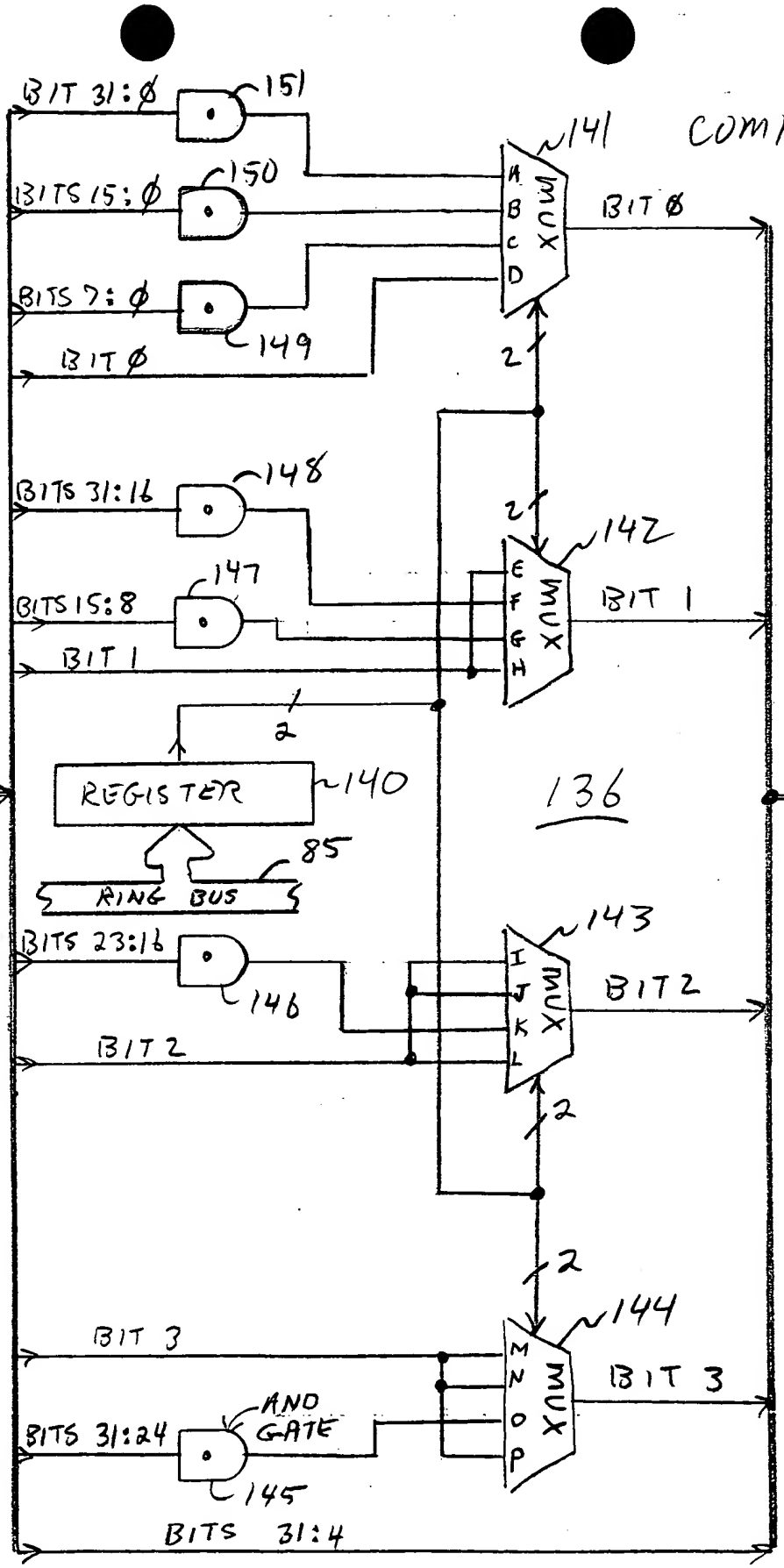

DATA CLASSIFIER (80-83)
132
133
134
135
DATA TO BE CLASSIFIED
IN
32
59/61
COMPRESSION
137
SHIFTING
138
MASKING
OUT
32
139
CLASSIFIED DATA
RING BUS
85

FIGURE 7


COMPRESSION (133)
BIT 31:0
151
BITS 15:0
150
BITS 7:0
149
BIT 0
141
MUX
A
B
C
D
BIT 0
2
TRUTH TABLE
MUX | REG. 140 = 00 | 01 | 10 | 11
141 | A | B | C | D
142 | E | F | G | H
143 | I | J | K | L
144 | M | N | O | P
165
BITS 31:16
148
BITS 15:8
147
BIT 1
142
E
F
G
H
BIT 1
2
REGISTER
140
136
137
32
32
RING BUS
85
59/61
BITS 23:16
146
BIT 2
143
I
J
K
L
BIT 2
2
2
BIT 3
144
M
N
O
P
BIT 3
BITS 31:24
AND GATE
145
BITS 31:4
DATA TO BE CLASSIFIED
COMPRESSED DATA TO BE SHIFTED
DOES
32 → 1
32 → 2
32 → 4
BUT
32 → 8
&
32 → 16
ARE NOT IMPLEMENTED
FIGURE 8
0067650 - 092800

SHIFTING (134)

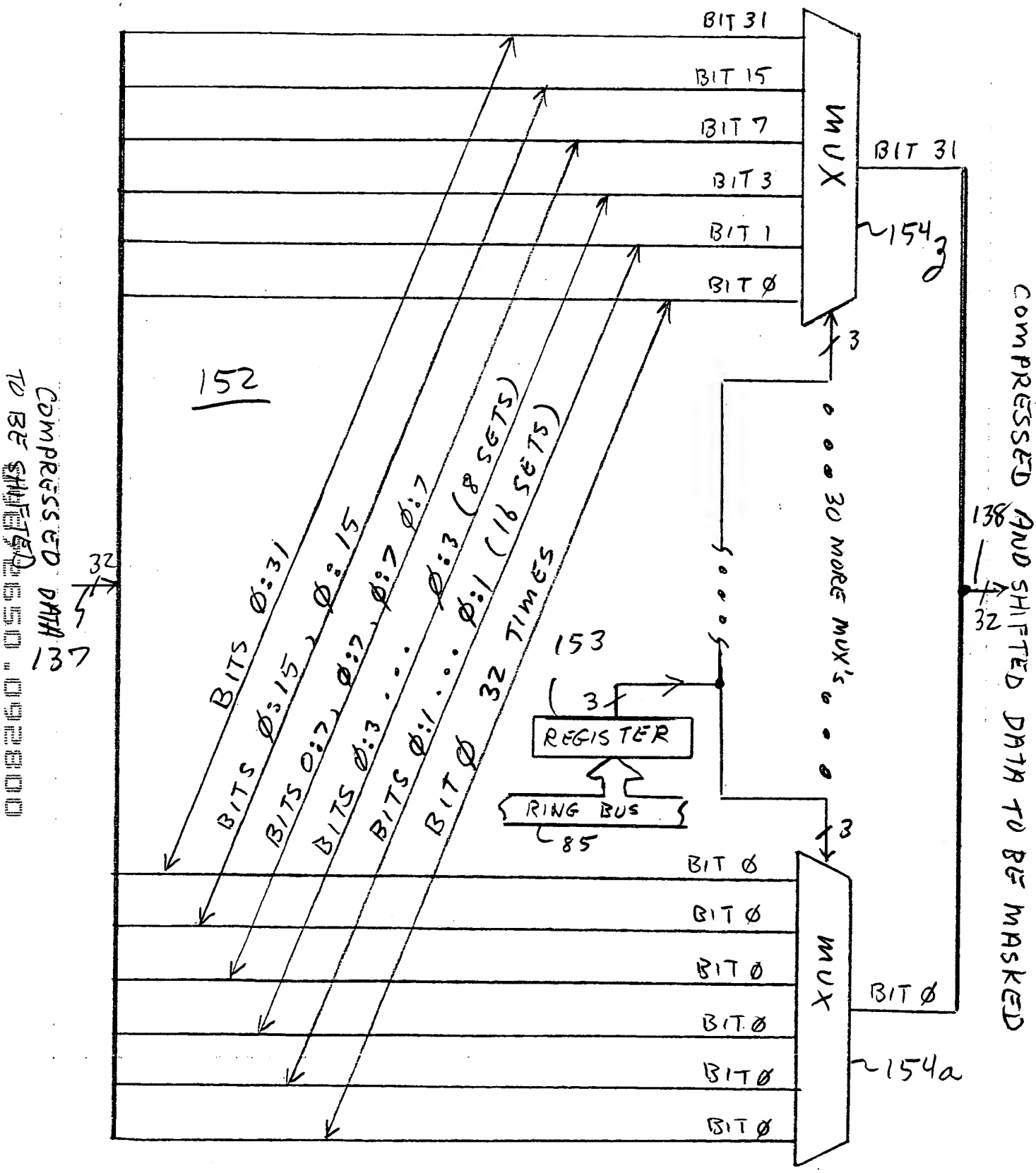


FIGURE 9

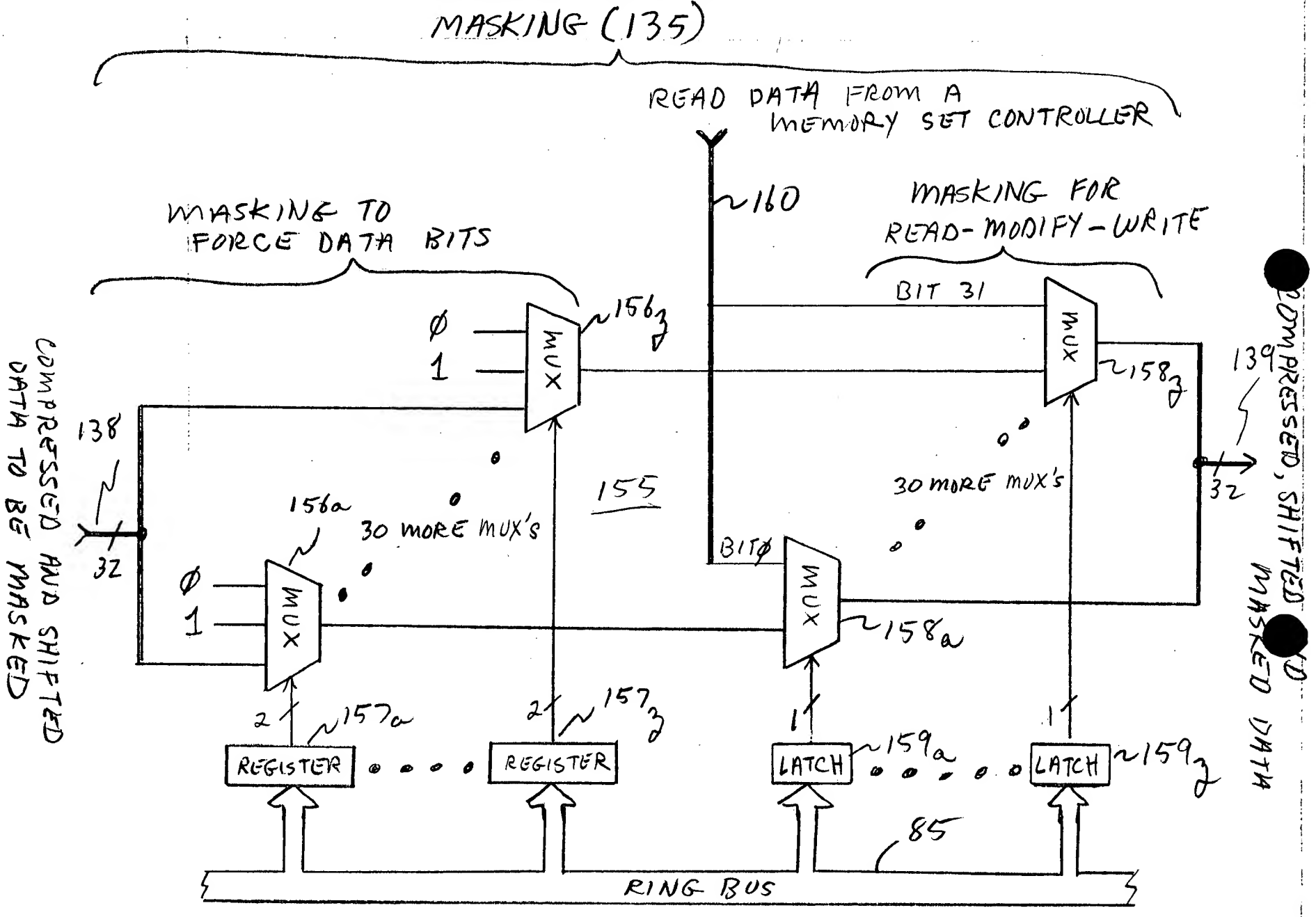

MASKING (135)
READ DATA FROM A MEMORY SET CONTROLLER
160
MASKING TO FORCE DATA BITS
MASKING FOR READ-MODIFY-WRITE
BIT 31
BIT 0
MUX
156
156a
158
158a
30 MORE MUX's
155
138
32
139
COMPRESSED AND SHIFTED DATA TO BE MASKED
COMPRESSED, SHIFTED AND MASKED DATA
REGISTER
157
157a
LATCH
159
159a
85
RING BUS

FIGURE 10

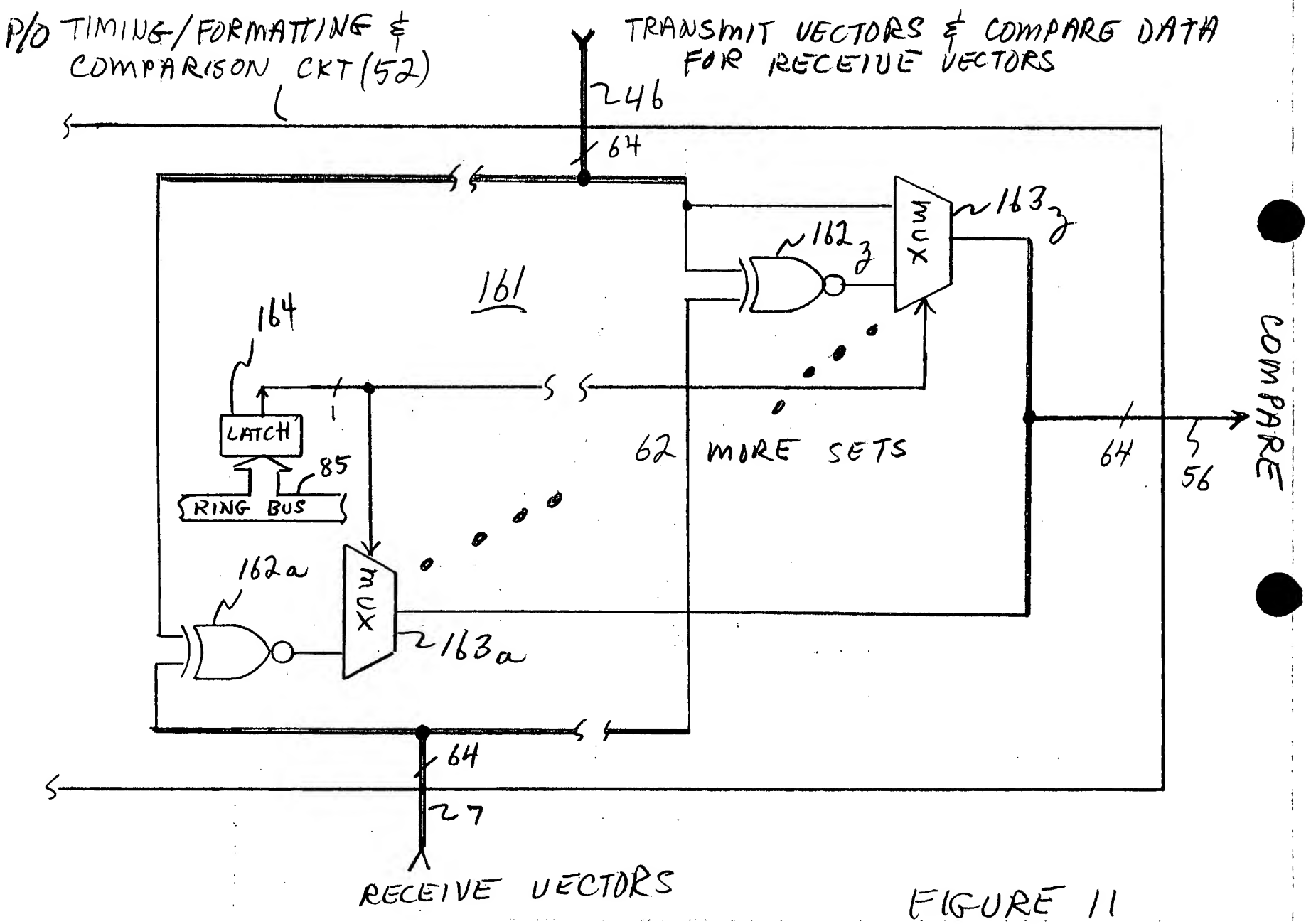

P/O TIMING/FORMATTING & COMPARISON CKT (52)
TRANSMIT VECTORS & COMPARE DATA FOR RECEIVE VECTORS
246
64
161
MUX
163
162
164
LATCH
RING BUS
85
1
62 MORE SETS
64
56
COMPARE
162a
163a
64
27
RECEIVE VECTORS

FIGURE 11